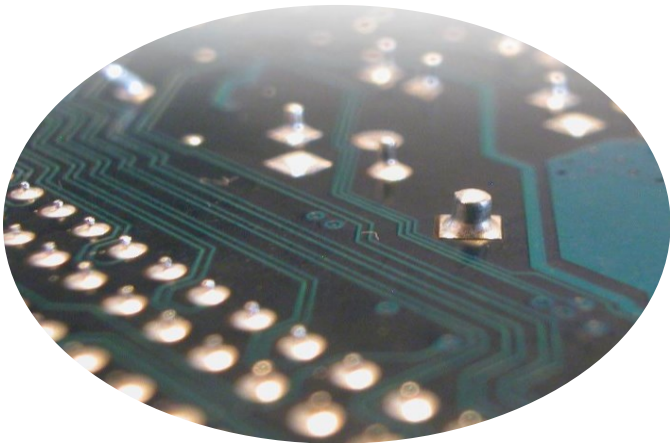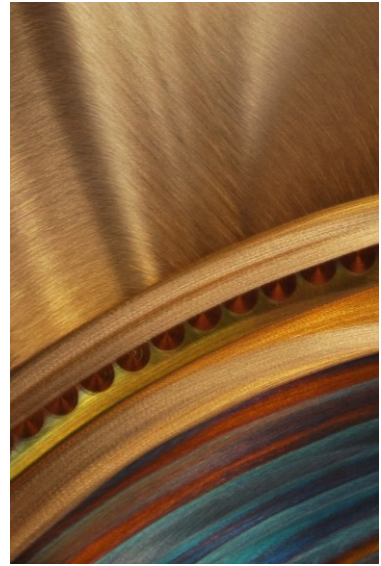# The TWO THINGS That Make Serial Links Work

…from 7 to 70 Gbps

Yes, just two things

Donald Telian

telian@siguys.com

SI GUYS

The TWO THINGS That Make Serial Links Work

Why DO serial links work? In this talk, Donald Telian explains that the two things that make links work are also the things that make them fail. When not done right. High-speed links work electrically when you (1) deliver 10 mV accuracy from Tx to Rx, and (2) properly equalize at the system level. As such, this talk details the primary technical requirements necessary to get these right. With tens of thousands of links in production, Telian has found serial technology to be quite robust. Indeed, when these basic things are done, the links have always worked right the first time. Nevertheless, when engineers do not do these two things, he gets the call. Uniquely positioning him to explain why serial links work, why they fail, and – most importantly – what you need to do in the design phase to make them work.

Donald Telian has worked in Signal Integrity for more than 40 years. For the last 20 years he has been a Consultant, focused on designing serial links into products from flash drives to switches with thousands of links. He has invented various SI concepts, tools, and quirks engineers use everyday to get their jobs done. He is an SI Coach, the owner of SiGuys.com, and the author of "Signal Integrity, In Practice" – a new book and in-person 2-day class that cuts through the noise to explain how to "do" SI when confronted with the data rates of today.

Signal Integrity, In Practice

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Before We Begin

Online Articles

- Time is limited today

- More info available in my book as shown here

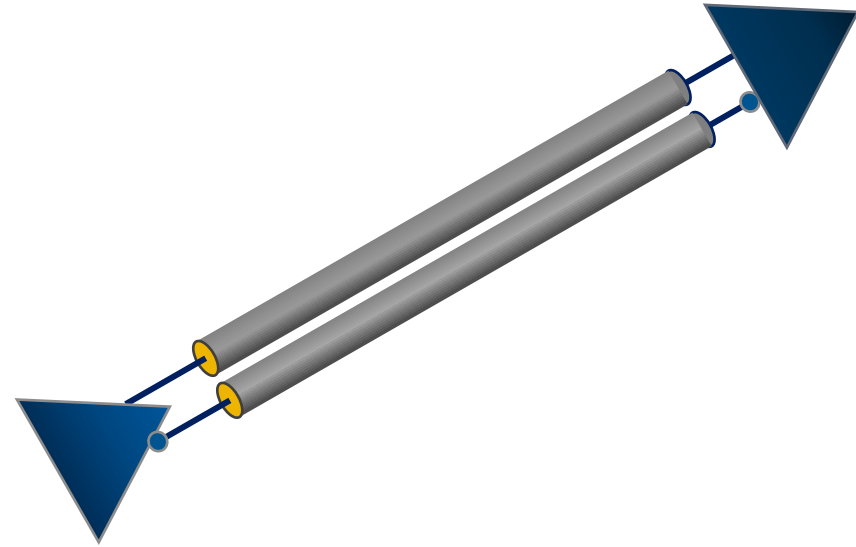- Even more info available at my **LIVE** workshops offered here:

Signal Integrity, in Practice

A **LIVE** 2-Day Workshop
With Donald Telian
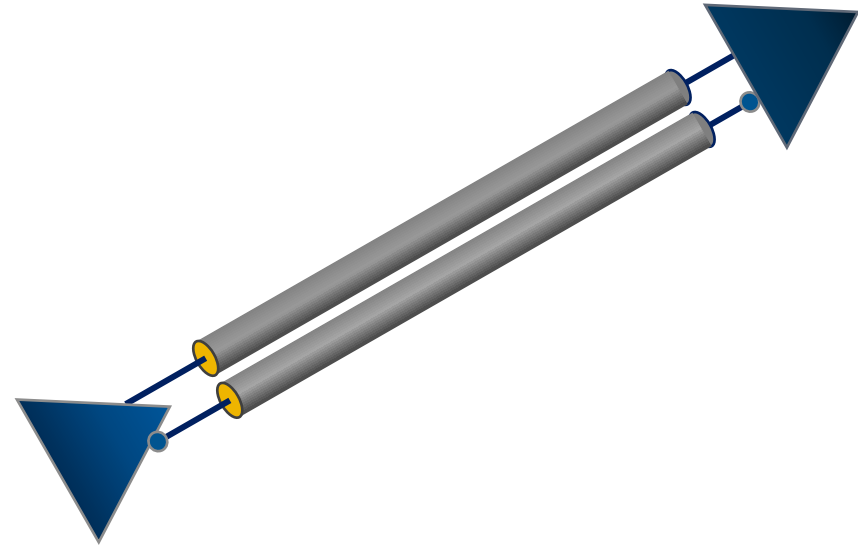SI Pioneer and Author

SI GUYS

Agenda:

1. Why Serial Links Work

2. Why Serial Links Fail

3. How to Make Links Work
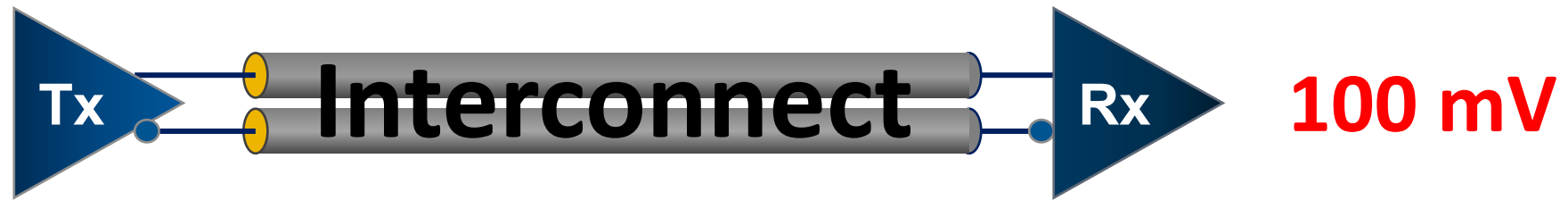
4. Welcome to Gen2 SI

SI GUYS

Agenda:

➡️ 1. Why Serial Links Work
- Two Reasons

2. Why Serial Links Fail

3. How to Make Links Work

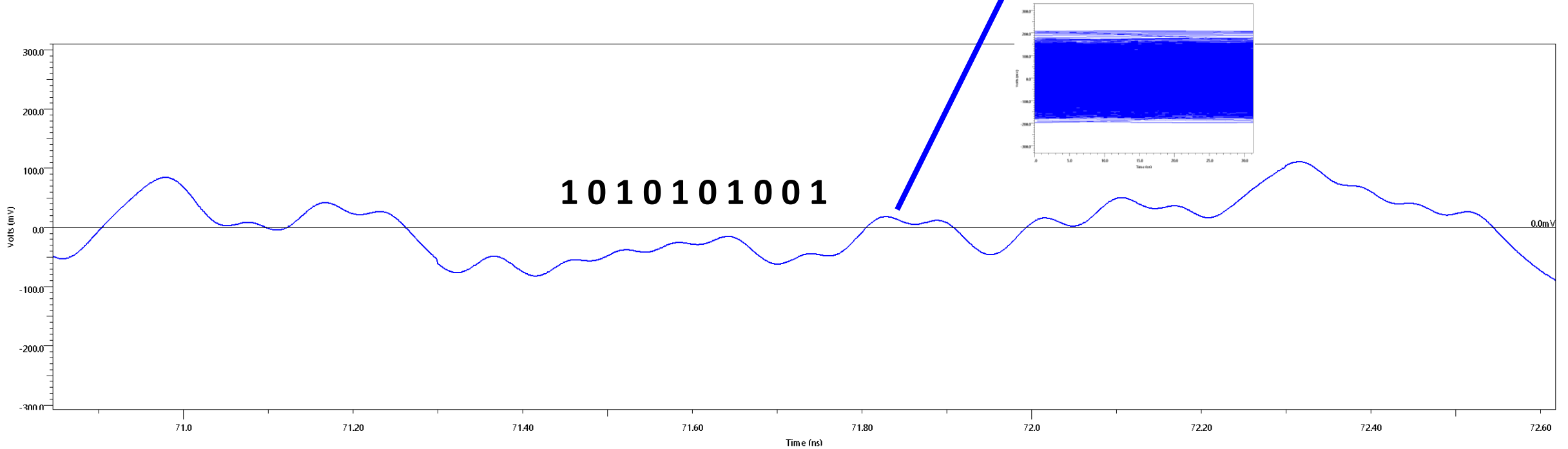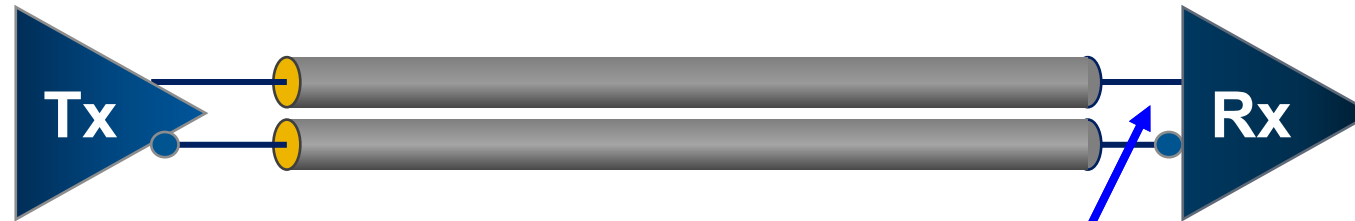4. Welcome to Gen2 SI

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A High-Speed Serial Link

1 V → ~40 dB Loss → 10 mV

Tx **Interconnect** Rx 100 mV

Transmitter (Tx), Differential Connection (Channel), Receiver (Rx)

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Why Serial Links Work, #1

Tx   **Rx**

1 0 1 0 1 0 1 0 0 1

Because we transmit across PCBs (passives) with 10mV accuracy

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Why Serial Links Work, #2

1 0 1 0 1 0 1 0 0 1
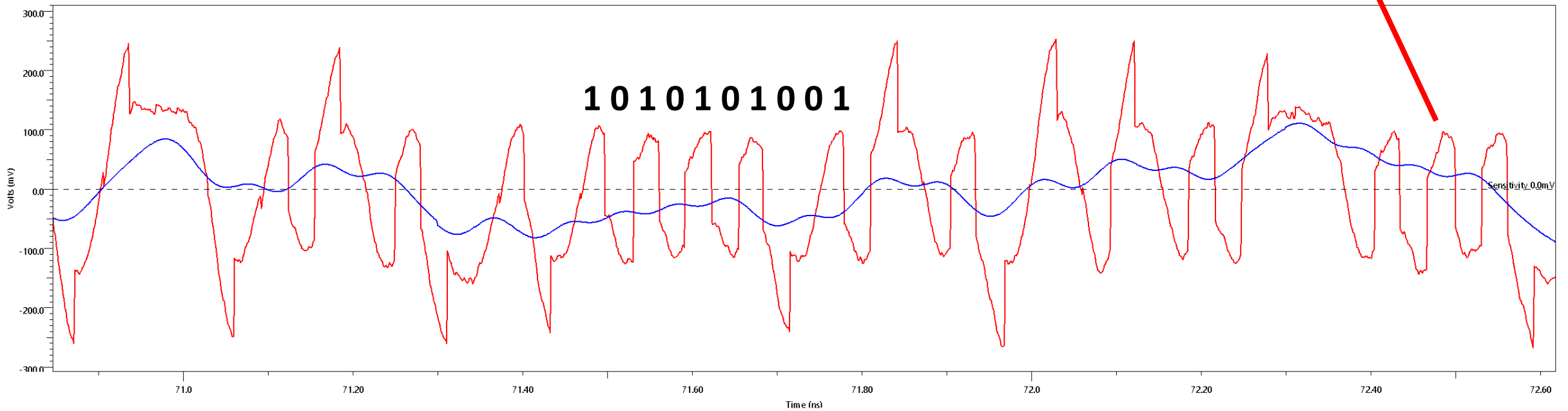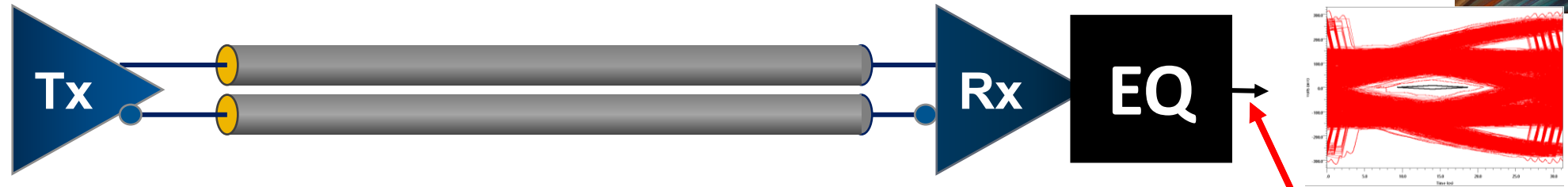
Because equalization (EQ) transforms our 10mV signals into logic levels

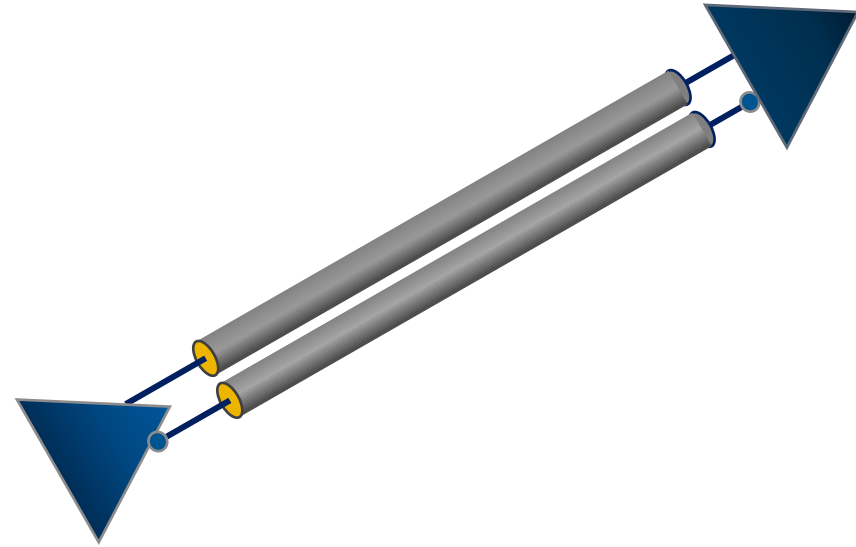Signal Integrity, In Practice

SI GUYS

Agenda:

1. Why Serial Links Work

2. Why Serial Links Fail

3. How to Make Links Work

4. Welcome to Gen2 SI

SI GUYS

Why Serial Links Fail?

*Not surprisingly, the **two reasons** why serial links **WORK** are also the **two reasons** why they **FAIL**:*

#1

INCORRECTLY CONFIGURED:

EQUALIZATION   (EQ)

Must recover the 100mV digital signal
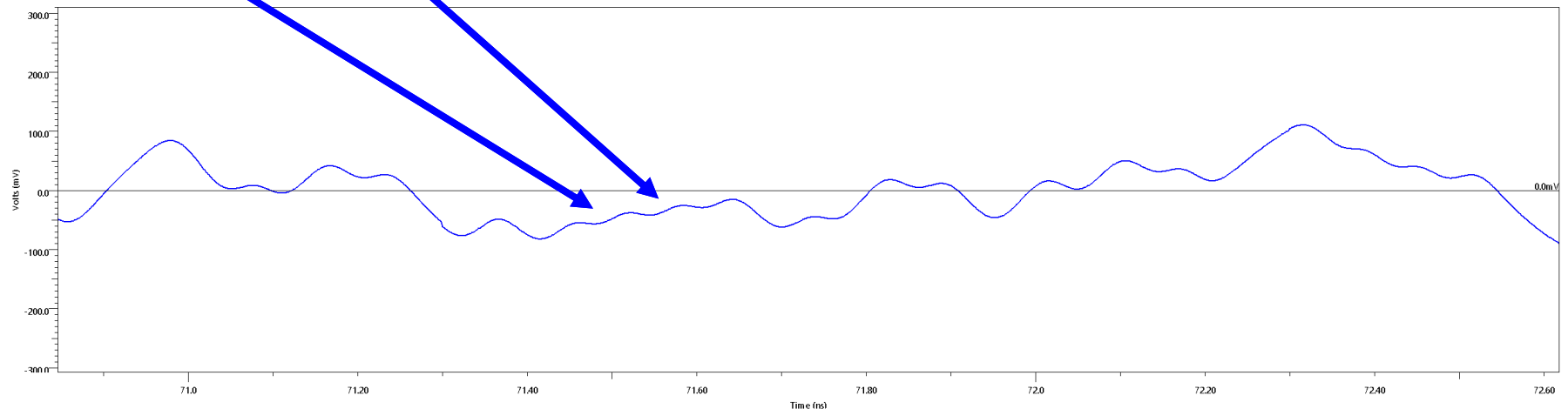
#2

INCORRECTLY MANAGED:

PASSIVE INTERCONNECT

Must preserve the 10mV analog signal

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Top THREE Reasons Why Serial Links Fail

1. Incorrectly Configured EQ
2. Discontinuities
3. Crosstalk

These two issues can cause 10+ mV signal perturbations that appear to the Rx as logic changes

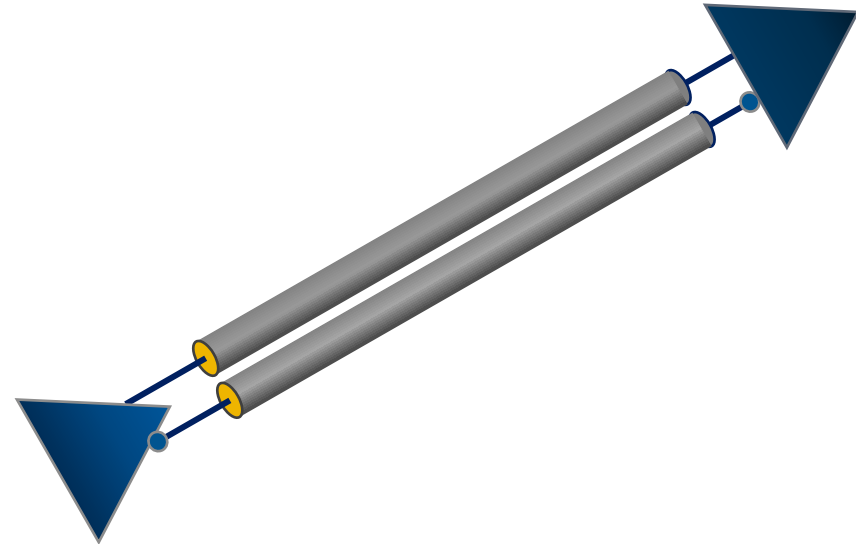Signal Integrity, In Practice

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Agenda:

1. Why Serial Links Work

2. Why Serial Links Fail

3. How to Make Links Work
   1. Configure EQ Correctly
   2. Minimize Discontinuities
   3. Control Crosstalk

4. Welcome to Gen2 SI

SI GUYS

#1: Configure EQ Correctly

EQ

- The Dream: ICs will optimize by themselves
  - This challenge is very complex
  - In practice, this doesn't work well. So what can be done?

- Step 1: Get access to Tx EQ software registers
  - You can do this!

- Step 2: Turn off Tx EQ
  - Sounds ridiculous? Oddly, this has solved many post-hardware serial link problems

Fix SI issues with Software

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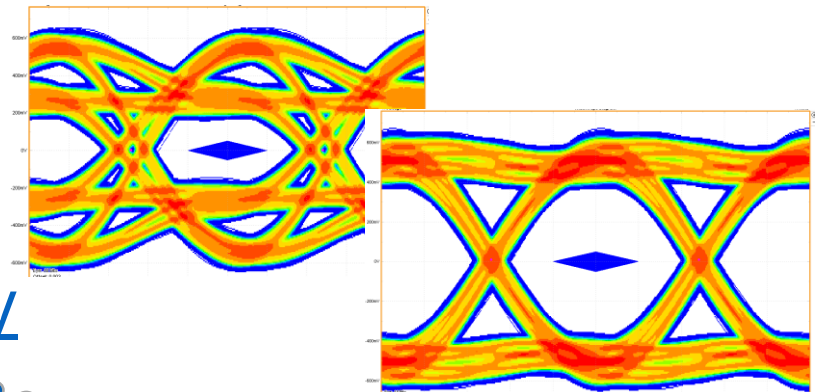
More EQ Detail

- Educate yourself on the EQ "Alphabet Soup" (acronyms)
  - CTLE, FFE, DFE, AGC, VGA, Taps/Cursors, CDR, etc.
  - These terms are as important as: stackup, return current, flight time…
- Rx EQ has become extremely powerful
  - Can handle much of the signal recovery problem by itself
    - And is typically self-optimizing (simpler, less of a system-level problem)
  - Redundant with Tx EQ, yet without amplitude penalty
    - And higher-loss systems must preserve amplitude!
- Use Tx for "pre-cursor" EQ
  - Something most Rx EQ cannot do

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Channel Pulse Response = Fingerprint

- Both **Loss** and **Discontinuities** close eyes
  - As colors show for two different channels
- Pulse response reveals what type of channel you have
  - And how to EQ/fix it!
- Great topic!
  - Hands on @ my SI Class
- Today's EQ handles **Loss** better than **Discontinuities**
  - *So design them out!*

Fingerprint Your Link

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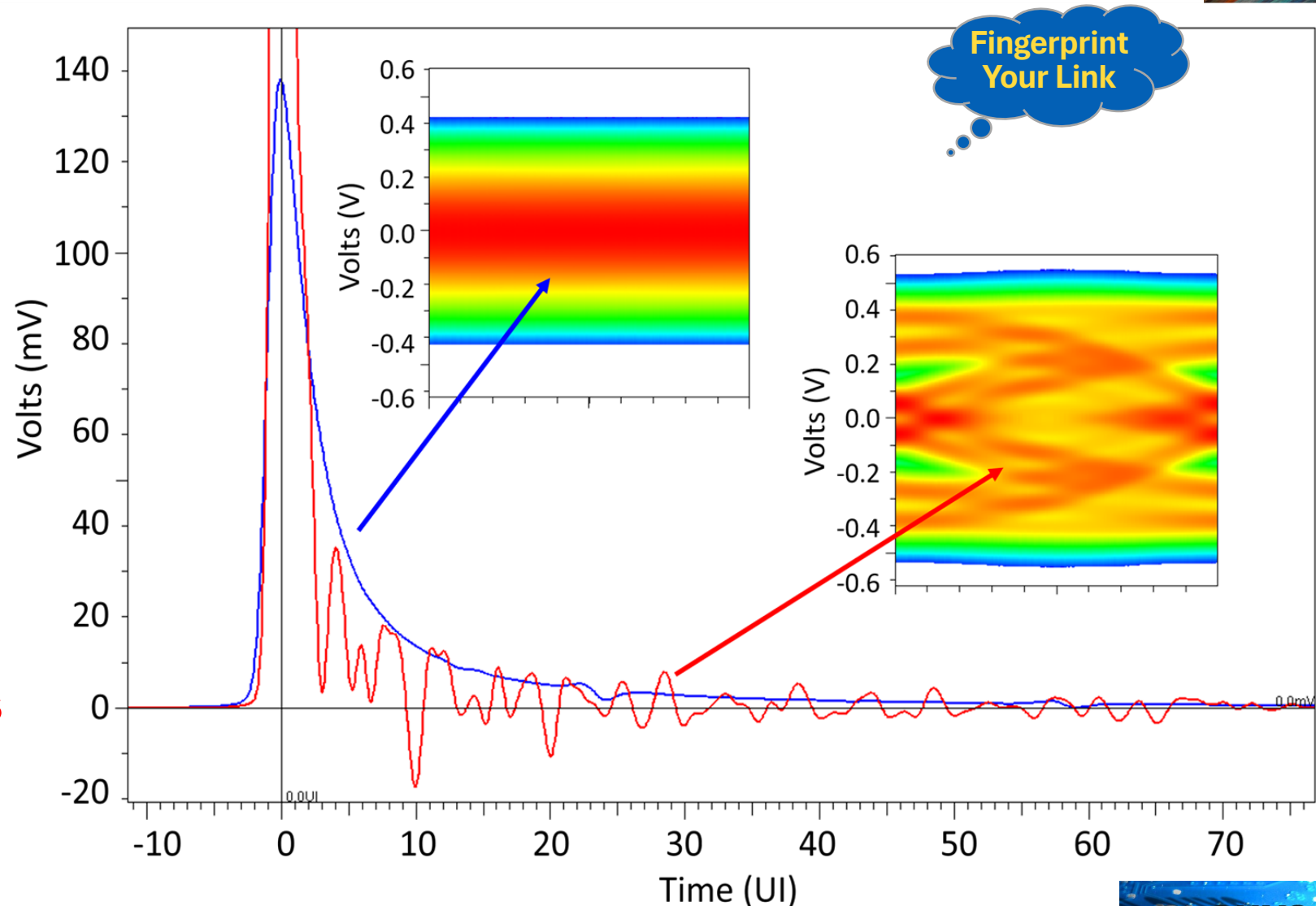
#2: Minimize Discontinuities
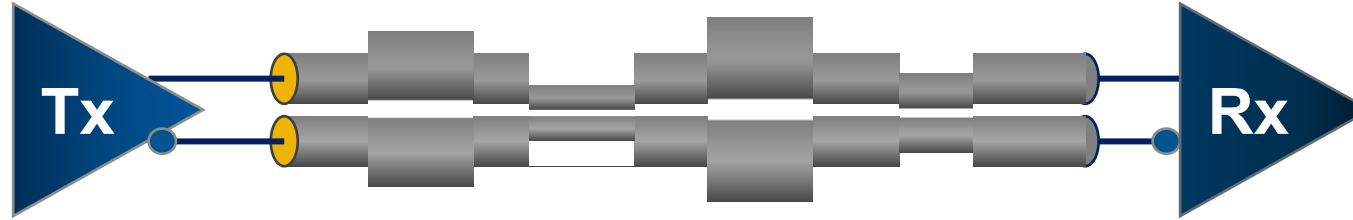
- In practice, a nice smooth connection from Tx to Rx doesn't exist
- Breakouts, AC capacitors, Connectors, Vias, etc. may present an impedance change
- Impedance changes cause signal "reflections" that damage SI

A "Discontinuity" occurs at any place in the connection
where the impedance changes

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Eight Ways To Fix a Discontinuity:

1. Ignore it   [Small Enough to Ignore?](#)

2. Remove it   [Step 1: Minimize Discontinuities](#)

3. Match it   [Understanding Via Impedance](#)

4. Equalize it   [Fixing SI Issues in Software](#)

5. Shorten it   [Fixing Stubs](#)

6. Distance it   [Discontinuity Proximity Effect](#)

7. Dampen it   [Trading Loss & Discontinuities](#)

8. Ground return it   [Proper Ground Return Vias](#)

Signal Integrity Journal

Home » Authors » Donald Telian

Donald Telian
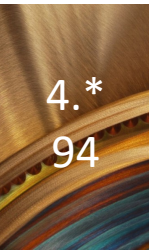
Discontinuities are the #2 problem - what I write about

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RFS = Which Discontinuites Matter
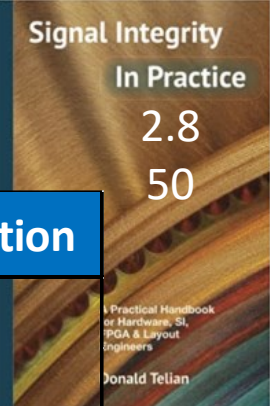
Feature	4 (5) Gbps	8 Gbps	16 Gbps	32 Gbps	64 Gbps	Unit	SIiP Section
Industry/PCIe terminology	Gen2	Gen3	Gen4	Gen5	Gen6		
Fundamental Frequency	2	4	8	16	16 (PAM4)	GHz	
Relevant Feature Size what's that?	160 traces	80 vias	40 conn pads	20 everything	20 everything	mils	4.1, 2.1, 4.x 4.2, 4.3, 4.4
Max Stub backdrills	64 none?	32 seq-lam	16 2 layers	8 per-layer	8 per-layer	mils	2.5, 1.3.3
P/N Matching, static	10	5	2	1	1	mils	2.3
Target Bit Error Ratio (BER)	1.E-12			1.E-06			
Route Style	45°	45°	curved	curved	curved		2.4
Diff-pair Spacing (XY/Z, min)	25	25	25	30	30	mils	5.3
Insertion Loss (max)	16	22	28	36	32	dB	2.2, 3.5
Min EQ: Tx_FFE/Rx_taps, CTLE	1 / 0	2 / 1, C	2 / 2, C	2 / 3, C	3 / 16, C+	#taps	3.3, 3.4, 2.7
Length-match method	serpentines		irregular spaced bumps				2.4
Fiberglass weave	spread glass and rotate image 12 degrees on panel						2.6
GND Return Vias (GRVs)	within 30 mils of signal layer transition						[48a, 3.2.2]
Solid GND reference layers	both sides of trace (don't use microstrips)						2.3, 2.6

2.8
50

that's my book →

"My SI Cheat Sheet"

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Find Discontinuities

Backplane

Tx Card

CONN

Rx Card

Reveals where discontinuities are, and their magnitude

Measurement TDR & VNA options

Simulators create this data too!
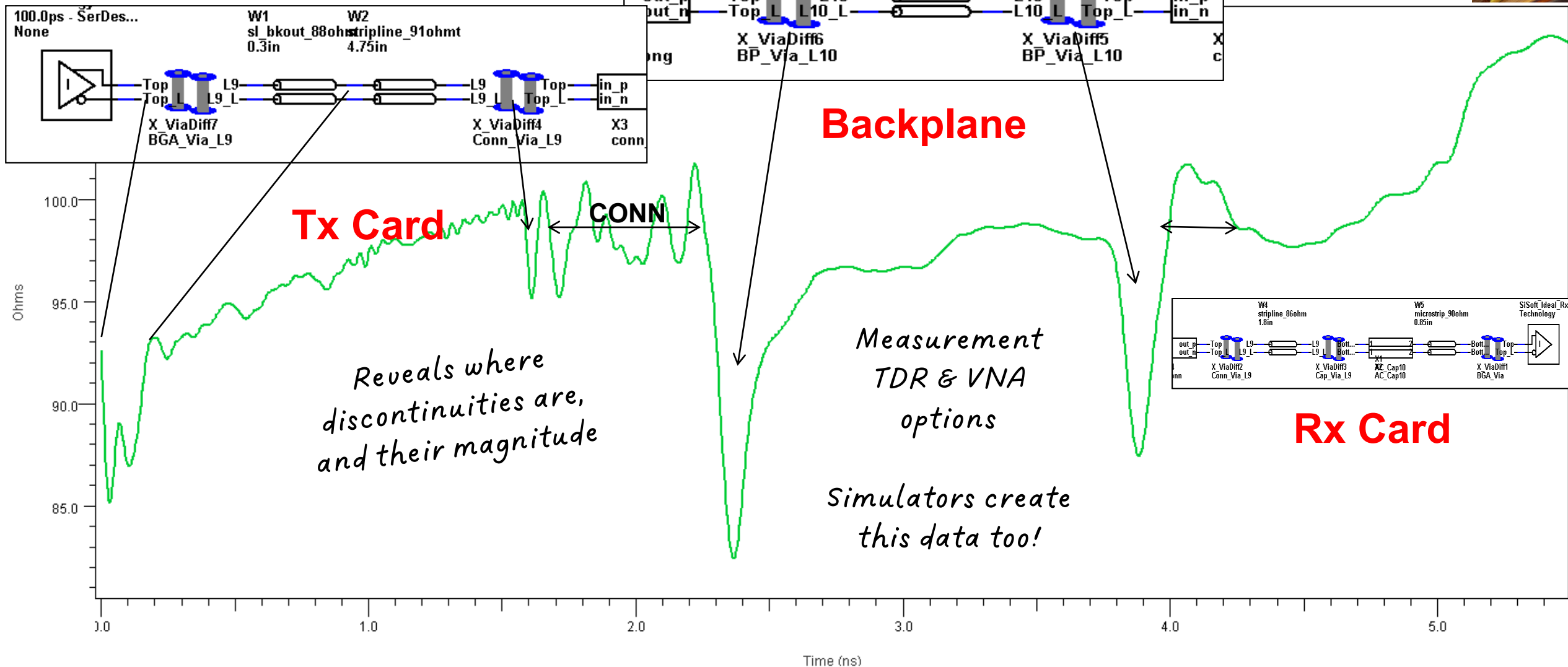
TDR is a great way to isolate & quantify discontinuities

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Stubs: Bad Discontinuities

- **Backdrill vias**
  - 8 to 16 Gbps failures

- **Remove stubs at solder pads**
  - 25 to 64 Gbps failures

- **Minimize stubs at edge fingers**
  - Should be handled by standard

Fixing the Problem of Stubs
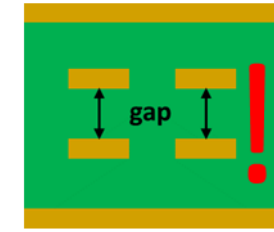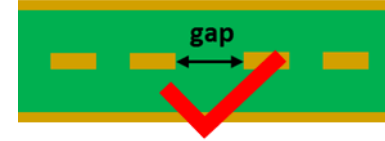
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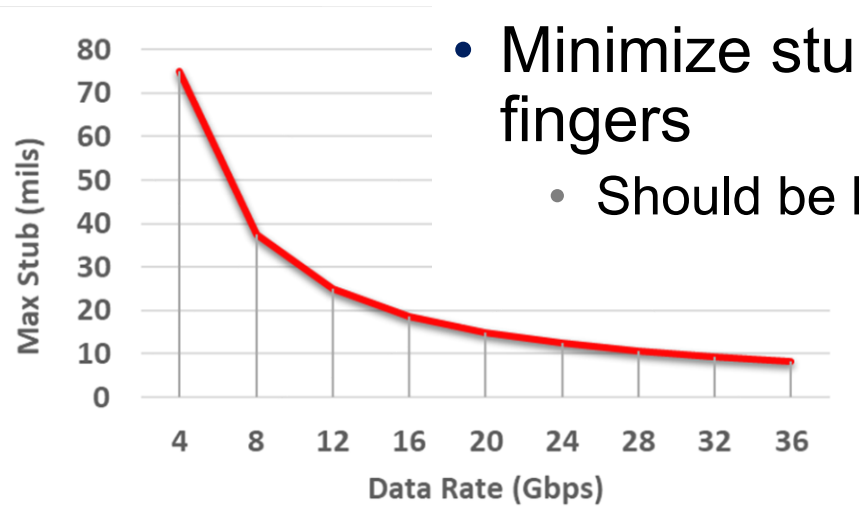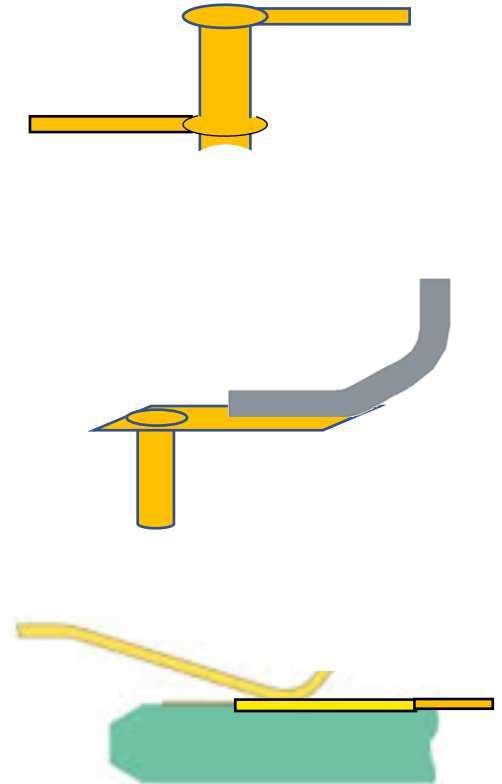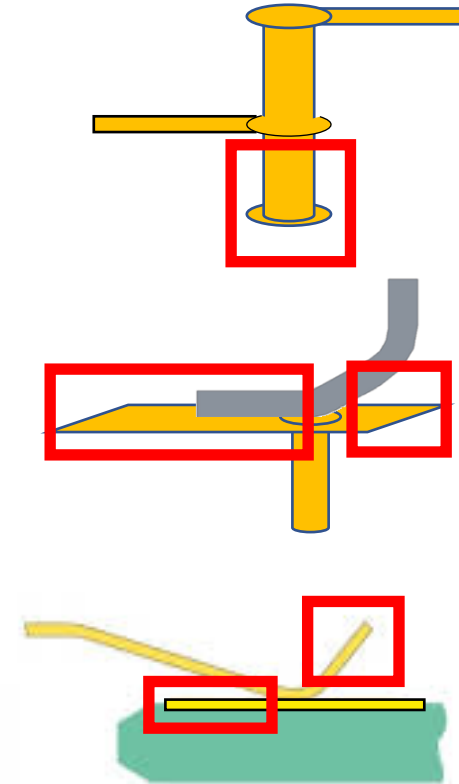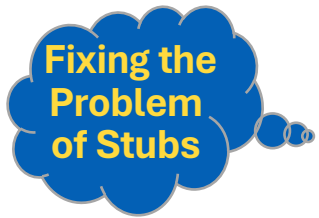
#3: Control Crosstalk

- Not where you expect
- Plane cutouts
  - Used to match impedance
  - Connector and Cap pads
- Cap Void Example
  - Near-end Tx (red)
  - Far-end Rx (blue)
  - Combined coupling = 120 mils
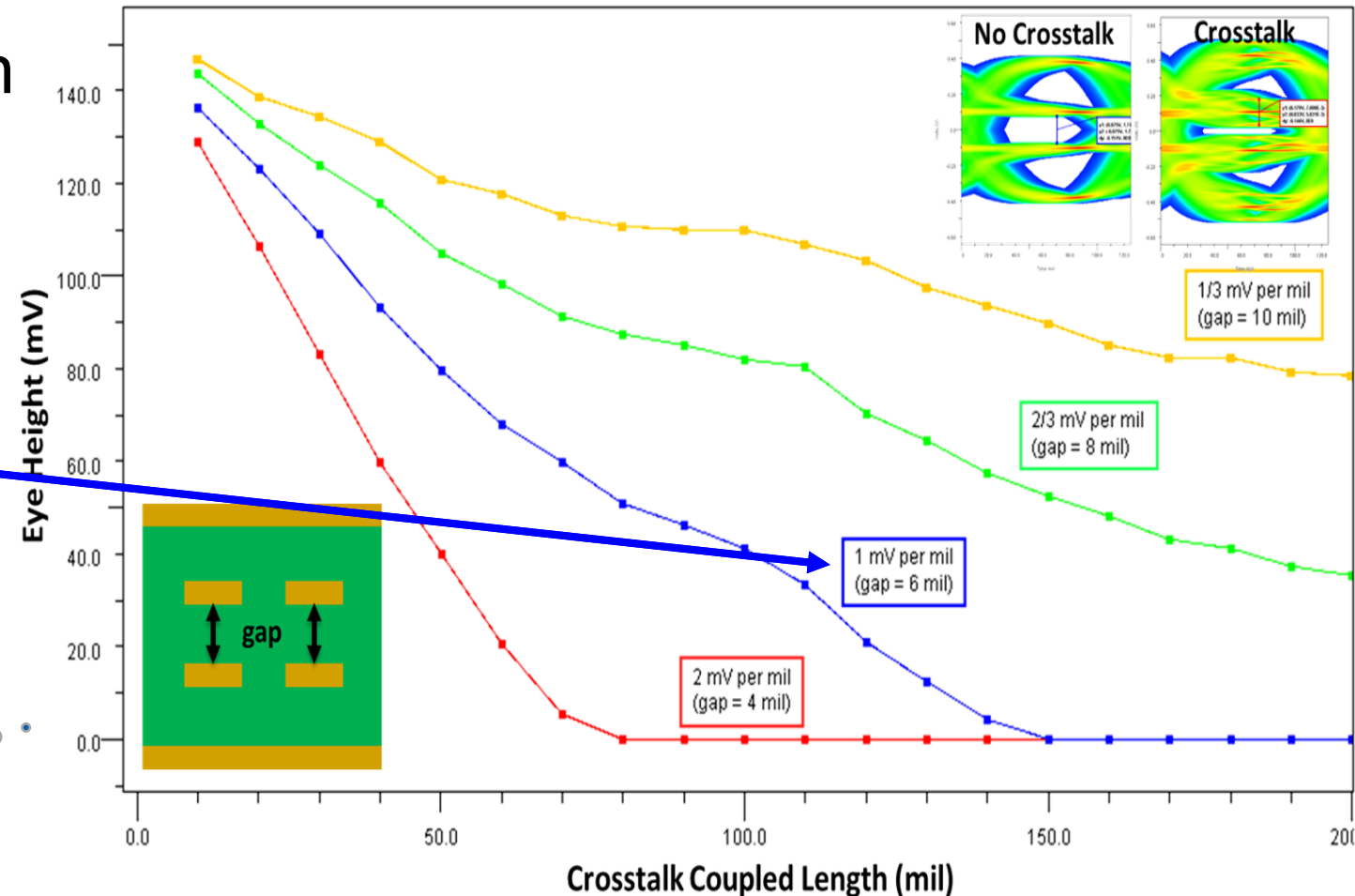- Always use route keepouts under voids, shields, 30+ mil gaps
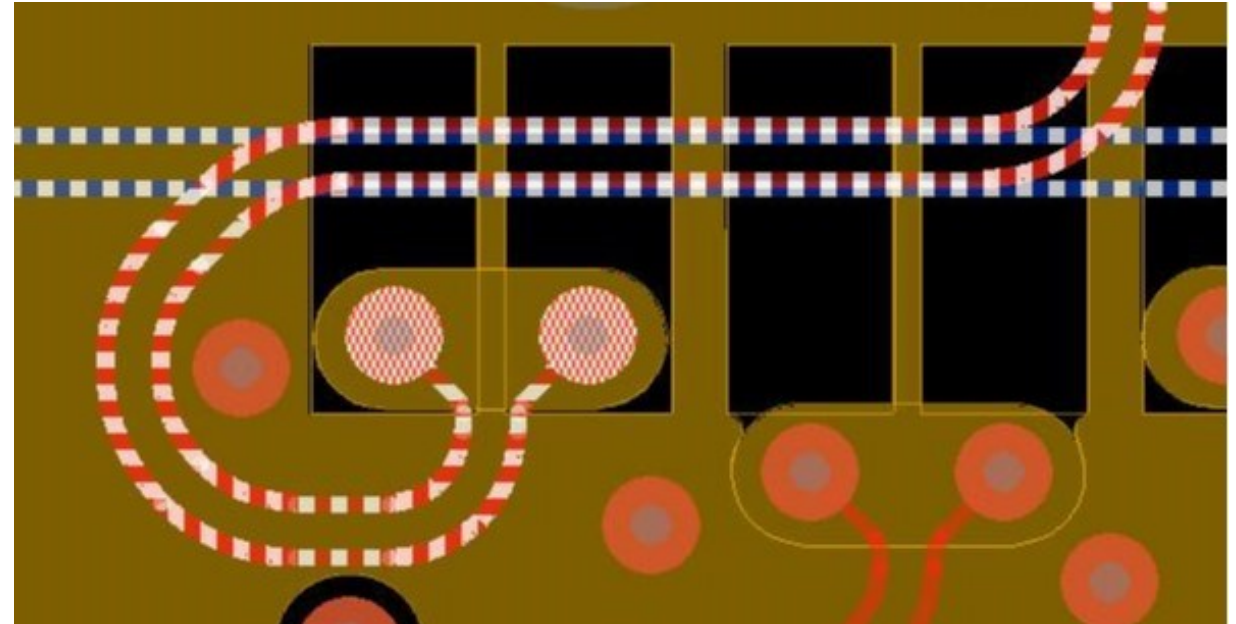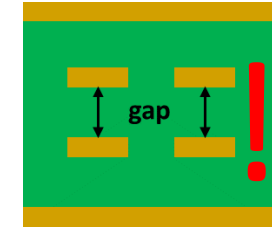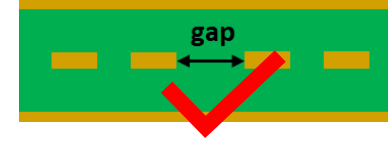
Best fix I've found is to visually check layer to layer

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10 mV Accumulates Fast!

- Eye height vs coupled length
  - Colors are gap distances

- 6 mil gap:
  - Typical PCB distance
  - 1 mV per 1 mil of coupling
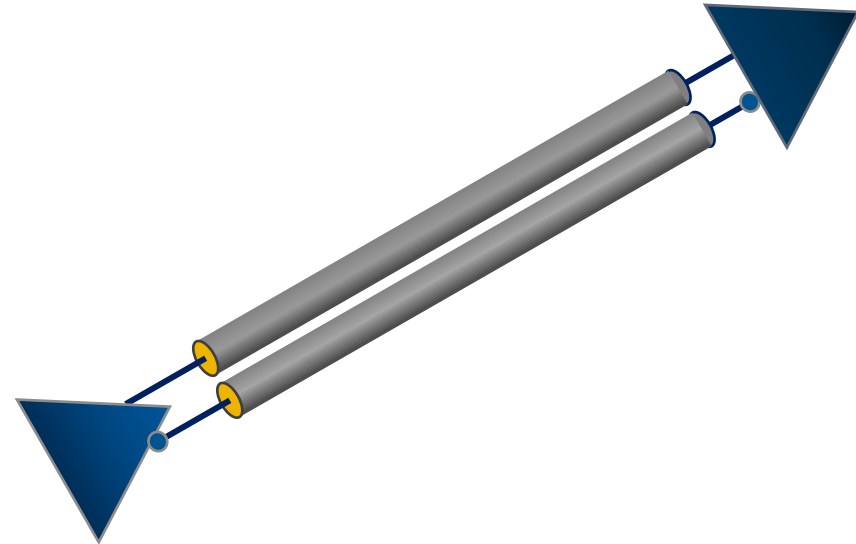 - Can close an eye

Managing PCB Crosstalk

1/3 mV per mil (gap = 10 mil)

2/3 mV per mil (gap = 8 mil)

1 mV per mil (gap = 6 mil)

2 mV per mil (gap = 4 mil)

No Crosstalk   Crosstalk

Signal Integrity, In Practice

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Agenda:

1. Why Serial Links Work

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3. How to Make Links Work

4. Welcome to Gen2 SI

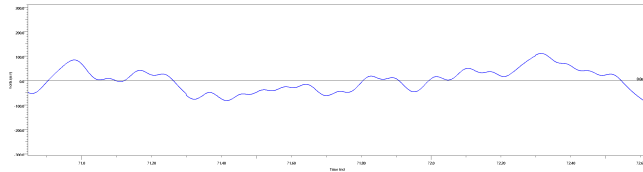Signal Integrity, In Practice

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Serial Links Define "High-Speed"

- Serial Links have changed the way we "do" signal integrity (SI)
  - I've simplified this new practice into "Gen2 SI"

- Serial revolution began in ~2001
  - Began at 1 Gigabits per second (Gbps), now 50+ Gbps

- 2002 Intel declares: cheaper to use transistors than PCB traces
  - Silicon integration becomes continual enabler of higher bandwidth
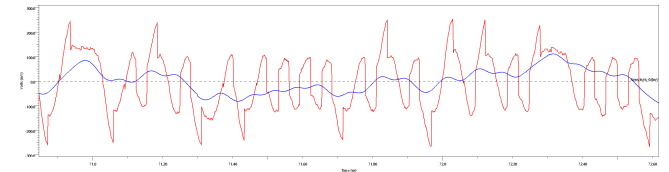
Silicon Integration Enabled Gen2 SI

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Signal Integrity   **SI**   **Silicon Integration**

Signal Integrity + Silicon Integration = SI + SI = Gen2 SI

Signal Integrity, In Practice

Technical Comparison

- ICs → 1,000,000x

- PCBs → 4x

- Data Rates → 5,000x

*In practice,
SI is simpler now
with Gen2 SI*

Gen1 Signal Integrity	Gen2 Signal Integrity
1986 to 2006	2007 to Present
Parallel	Serial
8 MHz to 3 GHz	4 to 70 GHz
System of ICs	IC dictates System
Mysterious "black magic"	Basic Science
Buffer VI/Slew	SerDes Equalization
Trace Length Rules	P/N Symmetry
Common & Source Clocks	Recovered Clock
AC Timings	Eye Diagrams, BER
Topology / Termination	Point-to-Point
Trace Impedance	Feature Impedance
Flight Time	Loss, Discontinuities
Ground Planes	Ground Returns/Grids
Stackup	Weave & Copper Profiles

SI GUYS

LIVE SI Class Teaching Tour!

- Munich Germany Oct 29 & 30 2025
  - In partnership with Zuken

- Private/Corporate Classes Too!

ZUKEN®

"out of the design cave"

Signal Integrity, in Practice

This is Gen2 SI

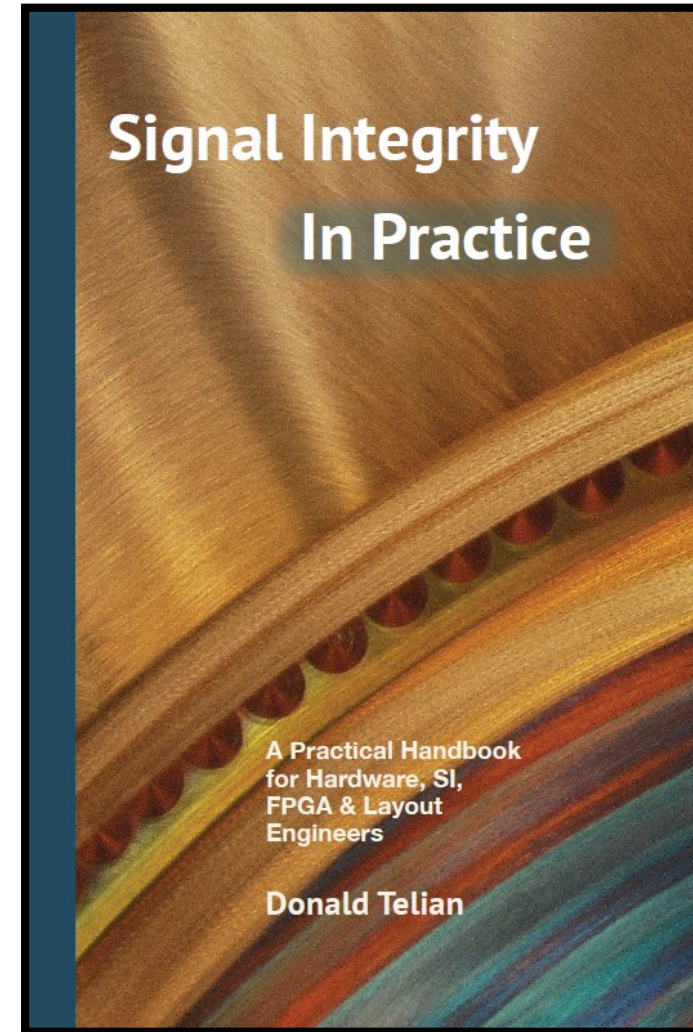A **LIVE** 2-Day Workshop
With Donald Telian
SI Pioneer and Author

https://siguys.com/training

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How I Can Help:

https://siguys.com/
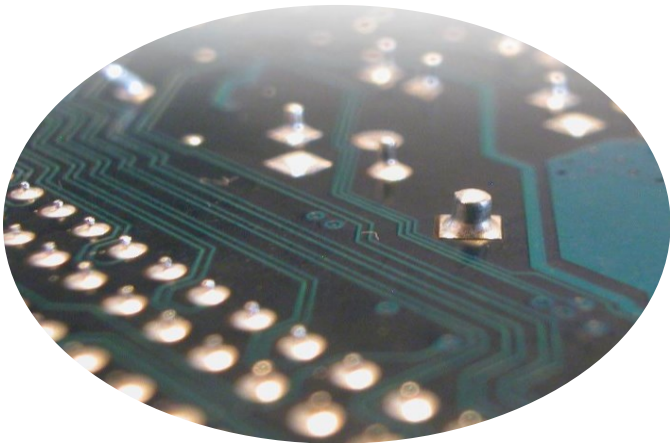

Available at Amazon

Hardcover or Kindle

THANK YOU

Let's achieve Signal Integrity, in Practice

Donald Telian

telian@siguys.com

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